EXPONENTIAL CHANNELIZED TIMER

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ABSTRACT OF THE DISCLOSURE

[0137] A multiprocessor switching device substantially implemented on a single CMOS integrated circuit is described in connection with a channelized timer for use in controlling the issuance of signals to the processor(s) or control logic (such as interrupts, descriptors, etc.) that that identify system-related functions for a plurality of channels. Using control registers to select an individual bit of a multi-bit counter, a timing interval pulse is provided for prompting signal generation that is otherwise subject to a minimum count requirement.